REMARKS

The applicants appreciate the acknowledgement of the claim for priority under section 119. The office action notes that a certified copy of the foreign priority application has not been filed. The certified copy of both priority applications was submitted on August 28, 2007, subsequent to the office action. A review of PAIR confirms that the certified copy of the priority applications are now of record. Accordingly, formal acknowledge of receipt of the certified copies of the priority documents is requested.

In addition, the applicants acknowledge receipt of the initialed copy of the form PTO 1449 filed on 26 February 2004.

Claims 1-16 are pending. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 1-16 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent No. 6,877,112, Iino ("Iino"). Claims 1-3 and 9-11 are amended. Support for the amendment is located in the application as filed, for example, page 8, lines 14-22; page 9, lines 13-20; and page 12, lines 9-11. Insofar as the rejection may be applied to the claims as amended, the applicants respectfully request that this rejection be withdrawn for reasons including the following, which are presented by way of example.

One aspect of the application mentions solving the problem of "correctly emulating an operation to be performed immediately after generation of a reset signal." (Specification page 3, lines 7-10.)

Claim 1 recites in combination, for example "a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address

instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal; and an interface circuit configured for performing input and output of information relating to emulation between the CPU and an external circuit, wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal." (See also independent claim 9.) Accordingly, the vector address switching circuit causes the CPU to execute different programs in accordance with different (first or second) reset signals, and the interface circuit is reset only by a second reset signal.

Without conceding that Iino discloses any feature of the present invention, Iino is directed to a reset control system and method. According to Iino, the first reset control section (605) OR-operates first and second reset signals; the OR operation result is output to the CPU core (604) as a first internal reset signal (629) for initializing the CPU core (604) (column 3, lines 55-63). A companion chip (606) has a second reset control section (607) which distributes the external reset signal (626) to a second internal reset signal (627) and second reset signal (628). (Col. 2, line 64 to Col. 3, line 2.)

The office action asserts that Iino discloses the invention as claimed. The office action refers to Iino, Col. 2 to Col. 3 as teaching a vector address switching circuit. To the contrary, Iino fails to teach or suggest the invention, as presently claimed, when the claims are considered as a whole. Iino fails to teach or suggest, for example, "a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU

when receiving a second reset signal." (See, e.g., claims 1, 9.) To the contrary, although Iino discloses different reset signals, Iino fails to teach or suggest anything about outputting different vector addresses to change programs to be executed by a CPU.

In the current independent claims 1 and 9, as compared with Iino, the vector address switching circuit outputs a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and outputs a different vector address (instead of the vector address corresponding to the reset vector address) when receiving a second reset signal. Furthermore, the vector address which is output "instead of the vector address corresponding to the reset vector address" is a "prescribed vector address."

Iino fails to teach or suggest, for example, these elements recited in amended independent claims 1 and 9. It is respectfully submitted therefore that claims 1 and 9 are patentable over Iino.

For at least these reasons, the combination of features recited in independent claims 1 and 9, when interpreted as a whole, is submitted to patentably distinguish over the references of record. In addition, Iino clearly fails to show other recited elements as well.

With respect to the rejected dependent claims, applicant respectfully submits that these claims are allowable not only by virtue of their dependency from independent claims 1 and 9, but also because of additional features they recite in combination.

Applicants respectfully submit that, as described above, the cited art does not show or suggest the combination of features recited in the claims. Applicants do not concede that the cited art shows any of the elements recited in the claims. However, applicants have provided specific examples of elements in the claims that are clearly not present in the cited art.

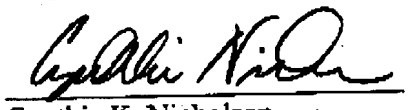
Applicants strongly emphasize that one reviewing the prosecution history should not interpret any of the examples applicant has described herein in connection with distinguishing

over the cited art as limiting to those specific features in isolation. Rather, for the sake of simplicity, applicants have provided examples of why the claims described above are distinguishable over the cited references.

In view of the foregoing, the applicants submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

Respectfully submitted,



Cynthia K. Nicholson
Reg. No. 36,880

Posz Law Group, PLC
12040 South Lakes Drive, Suite 101
Reston, VA 20191
Phone 703-707-9110
Fax 703-707-9112
Customer No. 23400